Remarks

This Amendment is responsive to the October 15, 2007 Office Action. Reexamination and reconsideration of **claims 1-6, 8-12, 14-18, and 20-24** is respectfully requested.

Summary of The Office Action

The 35 U.S.C. 112-second paragraph rejection of **Claim 11** was withdrawn due to amendments and remarks filed 12 July 2007.

The 35 U.S.C. 112-second paragraph rejections of **Claims 7, 8, 13, 19 and 20** were not withdrawn due to amendments and remarks filed 12 July 2007. These claims have been amended or cancelled as suggested in the Office Action.

The 35 U.S.C. 101 rejections of **Claims 11 and 22-24** were withdrawn due to amendments and remarks filed 12 July 2007.

Claims 7, 8, 13, 19 and 20 were rejected under 35 U.S.C. §112, second paragraph, for the presence of trademarks or trade names in the claims. These claims have been amended or cancelled as suggested in the Office Action.

Claims 1-9 and 14-24 were rejected under 35 U.S.C. §102(b) as being anticipated by Bhatia et al. (US 6,535,798 B1).

Claims 10 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia and general knowledge in the art.

Claims 11-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. and Hussain et al. (US 6,172,611 B1).

Rejections under 35 U.S.C. 112, second paragraph

Claims 7, 8, 13, 19 and 20 was objected to under 35 U.S.C. §112, second paragraph, for the presence of trademarks or trade names in the claims. These claims have been amended or cancelled as suggested in the Office Action.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §102

Claims 1-9 and 14-24 were rejected under 35 U.S.C. 102(b) as being anticipated by Bhatia. For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Bhatia is illustrated to be a conventional ACPI application that adds cyclic throttling in response to a signal from a processor that it is overheating. Bhatia discloses cyclic throttling to establish an ACPI state, not changing and maintaining a processor frequency and/or voltage in response to an operating system request by writing a set of bit patterns to a GPIO block whose address is stored in a data structure. Bhatia is a reactive system, the claims describe a proactive system.

The Office Action provides interpretations for the terms GPIO; register, set of bits, address, and frequency. The interpretation of GPIO is incorrect. The claims recite a "GPIO block", not just "GPIO". On page 6 of the Office Action, it is reported that the "Examiner has interpreted an 'I/O address space' as being the GPIO block." This is simply an incorrect interpretation.

The Office Action also provides an interpretation of "frequency". The Office Action asserts that "throttling a clock (stop/start) and increasing and/or decreasing the clock speed are equivalent". (Office Action, Page 11). This is incorrect for the

claimed invention with respect to heat creation and dissipation, and especially incorrect for amended claim 14. The Office Action asserts that alternately running a processor at 100Hz and then at 0Hz for equal periods of time produces 50Hz. While this may be logically attractive, it is incorrect when viewed in light of heat creation and dissipation. For this assertion to be true with respect to heat creation and dissipation, microprocessor heat production would have to be precisely linear with respect to frequency.

A flaw in the "frequency" interpretation can be seen by analogy to gas mileage. Consider the gas mileage of a car that averages 50 mph by alternating between 100 mph and 0 mph. Then consider the gas mileage of a car that averages 50 mph by establishing and maintaining 50 mph. The two situations would produce drastically different gas mileage. So too do running a processor substantially continuously at 50 Hz versus alternating between 100 Hz and 0 Hz. The 100Hz/0Hz model is cyclic throttling that happens in response to a processor overheating. The processor runs at 100Hz, the processor overheats, the processor sends a signal, the processor "runs" at 0Hz, the processor cools off, the processor runs at 100Hz, and so on. The constant 50Hz model is not cyclic throttling and is not initiated in response to a processor overheating. The 50Hz model runs continuously at the lower frequency after an operating system makes a request. The request may be made, for example, in response to a load determination.

Independent claim 1

Claim 1 recites a data structure that stores an address of a GPIO block and a set of bit patterns that may be written to the GPIO block or to a thermal management register. The reference does not disclose storing the address of the GPIO block or the set of bit patterns. While the reference may describe a power management module that stores the address of a register, which the Office Action interpretation of GPIO may support, the reference does not describe storing the address of a "GPIO block" as claimed. Bhatia merely describes creating a new performance state by writing a predefined value to a control register. (Bhatia, col. 12, lines 37-52). And

what is the effect of creating the new performance state? It is throttling by cycling between a high and low state. Consider that Bhatia discloses how G_STPCLK# may be used to perform processor clock throttling.

For the Office Action rejection to withstand scrutiny, "writing a predefined state to a control register" must be interpreted to disclose writing the bit pattern to the GPIO block. The Office Action asserts that having the control register defined in I/O address space equates to having a GPIO block whose address is stored in the claimed data structure. Applicant respectfully disagrees with this interpretation. Simply having a register defined in an I/O address space does not teach having an address for a GPIO block stored in the claimed data structure.

Bhatia describes a conventional ACPI approach to power management through register based clock throttling. The register based clock throttling does not include selecting a bit pattern and writing the bit pattern to the GPIO block. Instead, the register based clock throttling teaches placing a high or low voltage on a processor control line. Thus, Bhatia fails to teach each and every element of claim 1 and fails to establish a prima facie anticipation rejection. Since claim 1 recites features not taught or suggested by the reference, it patentably distinguishes over the reference. Accordingly, dependent claims 2-6 and 8-10 also patentably distinguish over the reference and are in condition for allowance.

Dependent Claim 2

This claim has been amended to include a limitation found in [0014]. This amendment makes clear that the thermal management action is taken in response to an operating system action rather than in response to a processor overheating signal from a processor. Bhatia teaches a system that throttles in response to a processor overheating, not an operating system initiated pre-emptive action. Since the claim includes elements not found in the reference, the claim patentably distinguishes over the reference and is in condition for allowance.

Dependent Claim 7

This claim has also been amended to include a limitation found in [0014] and to depend from claim 2. This amendment makes the request be initiated in response to a load determination. None of the references show this limitation since all of the references act in response to a processor overheating signal. Since the claim includes elements not found in the reference, the claim patentably distinguishes over the reference and is in condition for allowance.

Independent claim 14

Claim 14 is a method claim. This claim has been amended to add two limitations that are supported in the specification. The claim has been amended to include "maintaining" the frequency and voltage rather than "cyclic throttling". The claim has also been amended to require the bit pattern to include two or more bits. These additional limitations are supported in the specification and do not add new matter. Furthermore, these two limitations clearly distinguish over the cyclic throttling described in Bhatia. For these reasons this claim is not anticipated and is in condition for allowance.

Additionally, the original claim refers to "simulation data" that facilitates controlling the state of a thermal management signal and a thermal management register. While the reference describes storing the fact that an interrupt occurred in a single register bit (Col. 4, line 4-8), it does not describe storing simulation data. Simply recording the fact that something happened does not teach storing "simulation data" that can be used to do something about it. There is a difference between recording the fact that you were hit by a car in a hit and run accident and writing down the license plate so that the driver can be found. In one case, you have recorded the fact of your being hit while in the other you have stored data upon which an action can be taken. Since the reference does not teach the simulation data, for this additional reason this claim is not anticipated and is in condition for allowance.

The Office Action relies on Bhatia steps 304, 306, and 308 to support the assertion that the claim is anticipated. Step 304 teaches determining that a processor temperature exceeds a threshold. Step 306 teaches checking a processor state. Step 308 teaches transitioning a processor from a high performance state to a low performance state. These steps enable binary throttling to produce an actual processor state. These steps do not teach the claimed elements of "receiving a request", "accessing a data store", and "causing the processor performance state to be simulated."

Elsewhere, the Office Action argues that the SENSOR in figure 1 and receiving notification when a sensed temperature rises above a preset target teaches "receiving a request." This is incorrect. Receiving a notification that an event has occurred is not the same as receiving a request to do something. There is a difference between remarking that a pot is boiling over and receiving a request to remove the pot from the heat. Receiving notification of a fact (e.g., pot boiling over) is not the same as receiving a request to do something (e.g., remove pot). The Office Action appears to add the request to the notification. This is not supported by the reference. See also the amendments made to claim 15 that specifically address this notification issue.

The reference does not teach each and every element of the claim and does not make out a prima facie case for anticipation. Therefore this claim is in condition for allowance. Claims 15-18, and 20-21 depend from claim 14, which has been shown to be not anticipated by the reference. Thus, claims 15-18 and 20-21 are similarly not anticipated and are in condition for allowance.

Dependent Claim 15

This claim has been amended to include elements found in [0014]. The "request" is to be generated by an operating system in response to a load determination. The operating system does not have true processor states available. Since the claim includes elements not found in the reference, the claim patentably distinguishes over the reference and is in condition for allowance.

Independent Claim 22

Claim 22 is directed to a computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor. The method includes several actions, including receiving a request to establish the processor performance state in the processor, accessing a data store to acquire simulation data that facilitates controlling a state of a thermal management signal and a thermal management register, and causing the processor performance state to be simulated by causing the processor to set its operating frequency and operating voltage in response to the thermal management signal produced in response to writing a bit pattern to a GPIO block. The Office Action rejects claim 22 at page 11 using the same rationale as that applied to the system of claim 1. This is improper since the specific limitations of claim 22 have not been addressed.

For example, claim 22 refers to "simulation data" that facilitate controlling the state of a thermal management signal and a thermal management register. While the reference describes storing the fact that an interrupt occurred in a single register bit (Col. 4, line 4-8), it does not describe storing simulation data. Additionally, claim 22 claims causing a processor state to be simulated in response to writing a bit pattern to a GPIO block. Bhatia does not describe writing anything to a GPIO block, let alone a bit pattern than can cause a processor to change its frequency and voltage. For the rejection to stand, writing a single bit to a register having an address somewhere in the I/O space needs to be interpreted to anticipate writing a simulation data to a GPIO block. This interpretation is incorrect. Accordingly, Bhatia does not teach each and every element of claim 22 and therefore claim 22 is not anticipated and is in condition for allowance.

Independent claim 23

Claim 23 is a means plus function claim. The system includes means for accessing addresses and bit patterns that facilitate controlling a thermal

management signal available to a processor. The system also includes means for receiving a request to place the processor into a processor performance state and means for simulating a processor performance state. The Office Action rejects claim 23 at page 11 using the same rationale as that applied to the system of claim 1. This is improper since the specific limitations of claim 23 have not been addressed.

For example, claim 23 recites "means for receiving a request" Bhatia does not teach this element. The Office Action asserts that the SENSOR in figure 1 and notification when a sensed temperature rises above a preset target teaches "means for receiving a request." This is incorrect. Receiving a notification that an event has occurred is not the same as receiving a request to do something. There is a difference between being told by a stranger in the street that a building is on fire and having a fireman tell you to call 911 to ask that a fire truck be dispatched to the scene of a fire. Receiving notification of a fact (e.g., processor is hot) is not the same as receiving a request to do something (e.g., cool off processor).

Bhatia does not teach means for simulating the processor performance state by writing a bit pattern to a logic configured to control the thermal management signal. Thus, Bhatia fails to teach each and every element of the claim and the rejection should be withdrawn. Accordingly, claim 23 recites features not taught by the reference, it patentably distinguishes over the reference and is in condition for allowance.

Independent Claim 24

This claim is directed towards a set of application programming interfaces (API) embodied on a computer-readable medium for execution by a computer component. The API includes interfaces for communicating bit pattern data, GPIO bank address data, and state data. An API provides access to a system to programmers and/or processes. For example, a programmer can write a program to access a system through the API. An API encapsulates the functionality of a system while exposing the functionality. Specification at [0054]-[0055]. Bhatia discloses no

similar thing. Bhatia merely discloses an "interface" (e.g., register) that a power management module can write in a microprocessor. A register is not an API.

The Office Action asserts that Bhatia discloses an API because "the power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above." (Bhatia, col. 12, lines 29-31). Applicant respectfully submits that Bhatia does not teach an API. Nothing in the arguments provided on page 20 of the Office Action describe an API. Nothing in Bhatia describes an API.

The Office Action includes the statement that "applicant has only claimed an interface for communicating data between the system components." This is incorrect. Applicant asserts that the claims concern a "set of application programming interfaces". The Office Action is directed to specification paragraphs [0057] and [0058] and to figure 8 for the original description of how the API provides access to system functionality from outside the system. Upon such review, it becomes clear that claim 24 recites features not taught by the reference and is in condition for allowance. Withdrawal of this rejection is respectfully requested.

35 USC §103

Claims 10 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia and general knowledge in the art. To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143.01 Second, there must be a reasonable expectation of success. MPEP 2143.02 Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d

1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the criteria described in MPEP 2143.03 is not satisfied since the combination of references does not teach or suggest all the claim limitations. None of the references, alone and/or in combination, teach receiving a request to establish a desired processor performance state and thus claim 10 is not obvious over Bhatia and "general knowledge". Similarly, none of the references, alone and/or in combination, teach an API that facilitates simulating a processor performance state by applying a bit pattern to a GPIO block identified by a GPIO block address. Thus, claim 24 is not obvious over Bhatia and "general knowledge" for at least this reason.

Dependent Claim 10

Claim 10 depends from claim 1, which has been shown to be not anticipated, and therefore claim 10 cannot be obvious over the same reference. For this additional reason this claim is not obvious and is in condition for allowance.

Independent Claim 24

This claim is directed towards a set of application programming interfaces (API) embodied on a computer-readable medium for execution by a computer component. The API includes interfaces for communicating bit pattern data, GPIO bock address data, and state data. Using an API, a programmer can write a program to access a system. An API encapsulates the functionality of a system while exposing the functionality. Specification at [0054]-[0055].

The Office Action asserts that Bhatia discloses an API because "the power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above." (Bhatia, col. 12, lines 29-31). Applicant respectfully submits that Bhatia does not teach an API. Nothing in the arguments provided on page 20 of the Office Action describe an API.

The Office Action includes the statement that "applicant has only claimed an interface for communicating data between the system components." This is incorrect. The Office Action is directed to specification paragraphs [0057] and [0058] and to figure 8 for the original description of how the API provides access to system functionality from outside the system. Upon such review, it becomes clear that claim 24 recites features not taught by the reference and is in condition for allowance. Withdrawal of this rejection and/or a focused rejection of an API as claimed is respectfully requested.

Claims 11-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. and Hussain et al. (US 6,172,611 B1).

Independent claim 11

This claim recites a simulation logic to produce a simulated thermal management signal. The claim also recites a thermal management circuit that produces an actual thermal management signal. Thus the claim clearly recites producing two different signals. These are two signals that can be provided to a processor. The Office Action asserts that the simulated thermal management signal is taught by the power management module predefined values. Page 23. Additionally, the Office Action asserts that the "thermal management signal" is taught by the temperature sensor units providing a sampled temperature". Page 24. This is incorrect. The sampled temperature signal is provided from the processor to a control logic, not from a control logic to a processor. Thus, the sampled temperature cannot be the actual thermal management signal that is provided from the combination logic to the processor.

The claim recites that the combination logic can provide the actual thermal management signal or the simulated management circuit to the processor. A signal provided from the processor is not a signal provided to the processor and therefore the claim is not obvious over these signals. Bhatia only discloses providing a single signal, the actual thermal management signal.

The claim also recites a combination logic that can selectively provide either the actual signal or the simulated signal. Once again Bhatia only discloses providing an actual thermal management signal. The Office Action therefore relies on Hussain to provide the missing element. However, Hussain does not provide the missing signal. Instead, like Bhatia, Hussain describes receiving a system temperature signal. This signal flows into the logic, not out of the logic and in to the processor.

Neither reference describes choosing between an actual signal and a simulated signal because neither reference produces two signals. While both references may receive a temperature signal from a processor or other sensor, this temperature is not the "actual thermal management signal" that can be selectively provided to the processor by the combination logic. Thus, this rejection is without basis and should be withdrawn.

Since claim 11 recites features not taught by the references, it patentably distinguishes over the reference and is in condition for allowance. Accordingly, dependent claim 12 also patentably distinguishes over the references and is in condition for allowance.

Conclusion

For the reasons set forth above, **claims 1-6, 8-12, 14-18, and 20-24** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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